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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/291,006	04/14/1999	HIROKI HIYAMA	862.2789	1546

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EXAMINER	
HANNETT, JAMES M	

ART UNIT	PAPER NUMBER
2612	15

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/291,006	HIYAMA ET AL.	
	Examiner	Art Unit	
	James M Hannett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-24* is/are pending in the application.

4a) Of the above claim(s) *1-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14 and 18-24* is/are rejected.

7)☒ Claim(s) *16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 4/19/2004 have been fully considered but they are not persuasive. The applicants argument that the prior art does not teach the new limitations added to the claims is not persuasive. Nomura teaches in Figures 16 and 17 and teaches on Column 39, Lines 40-67 that driving circuits adapted to reset output lines, both reset lines can be reset using reset lines RG and RSV. Nomura teaches transferring to the output lines (202a) first signals obtained from the field effect transistors (QA) by resetting the gates of the field effect transistors (QA); As depicted in Figure 17, the signals are output from the field effect transistor (QA) by first resetting the gate of the field effect transistor, this occurs in time period T10-T11, Then the signal is output by driving (TG) low in time period T14. Nomura teaches turning on the first switches (TR) and reset the output lines (202a) while transferring the photo-charge to the gates of the field effect transistors (QA). As depicted from the timing diagram in Figure 17, the reset gate (TR) for the output line (202a) is activated in time periods (T13-T15). Furthermore, Gate (TG) is activated at time period (T14). This causes the photo-charge from the Photodiode (PD) to be transferred to the gates of the field effect transistor (QA) while the output line (202a) is being reset. Furthermore, Normura teaches in time period (T17) that the readout gate (QT) is activated which causes the photo-charge to be output to the gate of the field effect transistor (QA) and output to the output line (202a). This is viewed by the examiner as the transfer of a second signal from the field effect transistors (QA) to the output lines (202a).

Election/Restrictions

Applicant's election of Claims 14-24 in Paper No. 7 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1: Claims 14, 19, 20, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,933,189 Nomura in view of USPN 5,808,677 Yonemoto.

2: As for Claim 14, Nomura teaches in Figure 16 and on Column 38, Lines 1-17 a solid state image sensing apparatus comprising: a plurality of pixels each including a photoelectric conversion element (PD), a field effect transistor (QA) whose gate receives photo-charge generated by the photoelectric conversion element, a first switch (QT) for controlling connection between the photoelectric conversion element and the gate of the field effect transistor, and a first reset means (QP) for resetting the gate of the field effect transistor; Output lines (202a) for transferring an output from the field effect transistors; Column 38, Lines 18-27; Load means (212a), provided on the output lines, for the field effect transistors, Column 39, Lines 18-25; and second reset means (TR) for resetting the output lines to a predetermined voltage.

Nomura teaches in Figures 16 and 17 and on Column 39, Lines 40-67 that driving circuits adapted to reset output lines, both reset lines can be reset using reset lines RG and RSV. Nomura teaches transferring to the output lines (202a) first signals obtained from the field effect

transistors (QA) by resetting the gates of the field effect transistors (QA); As depicted in Figure 17, the signals are output from the field effect transistor (QA) by first resetting the gate of the field effect transistor, this occurs in time period T10-T11, Then the signal is output by driving (TG) low in time period T14. Nomura teaches turning on the first switches (TR) and reset the output lines (202a) while transferring the photo-charge to the gates of the field effect transistors (QA). As depicted from the timing diagram in Figure 17, the reset gate (TR) for the output line (202a) is activated in time periods (T13-T15). Furthermore, Gate (TG) is activated at time period (T14). This causes the photo-charge from the Photodiode (PD) to be transferred to the gates of the field effect transistor (QA) while the output line (202a) is being reset. Furthermore, Normura teaches in time period (T17) that the readout gate (QT) is activated which causes the photo-charge to be output to the gate of the field effect transistor (QA) and output to the output line (202a). This is viewed by the examiner as the transfer of a second signal from the field effect transistors (QA) to the output lines (202a).

Nomura teaches that the predetermined voltage is ground voltage; Column 39, Lines 18-25. However, Nomura does not teach a method for resetting the output line to a voltage other than a ground voltage.

Yonemoto depicts in Figure 12 and teaches on Column 10, Lines 55-67, Column 11, Lines 63-67 and Column 12, Lines 1-9 The method of resetting an output line (5) to a voltage (Vrb) that is not equal to a ground voltage. Yonemoto teaches that it is advantageous to be able to control the reset voltage because it can reduce the jitter component and can readily stabilize the signal voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the output line of Nomura to be reset to a voltage other than a ground voltage as taught by Yonemoto in order to reduce the jitter component and readily stabilize the signal voltage.

3: In regards to Claim 19, Nomura further teaches in Figure 7 the use of each pixel comprising a fourth switch (QB), arranged between the field effect transistor (QA) and the output line, adapted to select a row; Column 21, Lines 1-20 Nomura teaches that the signal will be output to the output line through the switch (QB) when The switch is turned on by a voltage VB. Therefore, because the signal in the given row will only be output when the transistor (QB) is on it performs a function of selecting the row.

4: As for Claim 20, Nomura teaches in Figure 16 and on Column 38, Lines 1-17 a method of operating a solid-state image sensing apparatus having pixels each including a photoelectric conversion element (PD), a field effect transistor (QA) whose gate receives photo-charge generated by the photoelectric conversion element, a first switch (QT) adapted to control connection between the photoelectric conversion element and the gate of the field effect transistor, and a first reset (QP) circuit adapted to reset the gate of the field effect transistor, and output lines (202) adapted to transfer an output from the field effect transistor, Column 38, Lines 18-27; loads (212), provided on the output lines, for the field effect transistors, Column 39, Lines 18-67; and second reset (TR) circuit adapted to reset the output lines to a predetermined voltage, said method comprising:

Nomura teaches in Figures 16 and 17 and on Column 39, Lines 40-67 that driving circuits adapted to reset output lines, both reset lines can be reset using reset lines RG and RSV. Nomura

teaches transferring to the output lines (202a) first signals obtained from the field effect transistors (QA) by resetting the gates of the field effect transistors (QA); As depicted in Figure 17, the signals are output from the field effect transistor (QA) by first resetting the gate of the field effect transistor, this occurs in time period T10-T11, Then the signal is output by driving (TG) low in time period T14. Nomura teaches turning on the first switches (TR) and reset the output lines (202a) while transferring the photo-charge to the gates of the field effect transistors (QA). As depicted from the timing diagram in Figure 17, the reset gate (TR) for the output line (202a) is activated in time periods (T13-T15). Furthermore, Gate (TG) is activated at time period (T14). This causes the photo-charge from the Photodiode (PD) to be transferred to the gates of the field effect transistor (QA) while the output line (202a) is being reset. Furthermore, Normura teaches in time period (T17) that the readout gate (QT) is activated which causes the photo-charge to be output to the gate of the field effect transistor (QA) and output to the output line (202a). This is viewed by the examiner as the transfer of a second signal from the field effect transistors (QA) to the output lines (202a).

Nomura teaches that the predetermined voltage is ground voltage; Column 39, Lines 18-25. However, Nomura does not teach a method for resetting the output line to a voltage other than a ground voltage.

Yonemoto depicts in Figure 12 and teaches on Column 10, Lines 55-67, Column 11, Lines 63-67 and Column 12, Lines 1-9 The method of resetting an output line (5) to a voltage (Vrb) that is not equal to a ground voltage. Yonemoto teaches that it is advantageous to be able to control the reset voltage because it can reduce the jitter component and can readily stabilize the signal voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the output line of Nomura to be reset to a voltage other than a ground voltage as taught by Yonemoto in order to reduce the jitter component and readily stabilize the signal voltage.

5: In regards to Claim 23, Nomura further teaches in Figure 7 the use of comprising a fourth switch (QB), arranged between the field effect transistor (QA) and the output line, adapted to select a row; Column 21, Lines 1-20 Nomura teaches that the signal will be output to the output line through the switch (QB) when The switch is turned on by a voltage VB. Therefore, because the signal in the given row will only be output when the transistor (QB) is on it performs a function of selecting the row.

6: As for Claim 24, Nomura teaches that the photoelectric conversion element is a photodiode (PD), Column 40, Lines 1-32. Furthermore, the photodiode is depleted after the transference of the photo-charge from the photoelectric conversion element to the gate of the field effect transistor, Column 14, Lines 44-63.

7: Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,933,189 Nomura in view of USPN 5,808,677 Yonemoto in view of USPN 6,538,693 Kozuka.

8: In regards to Claim 21, Nomura in view of Yonemoto teaches the claimed invention as discussed above in Claim 20. However, Nomura does not teach the method of outputting the signal from the pixels through switches to storage capacitors.

Kozuka teaches in Figure 1A and on Column 4, Lines 65-67; and Column 5, Lines 1-30 that it is advantageous to output the signals from pixels in an image sensor array to a noise signal removing unit in order to improve the image quality. Furthermore, this circuit includes a first

capacitor (9) and a second capacitor (10) connected to each of the output lines, a second switch (7) for controlling connection between the output line and the first capacitor (9), and a third switch (8) for controlling connection between the output line and the second capacitor (10), further comprising the steps of: Transferring the first signal, outputted from the field effect transistor reset by the first reset means, to the first capacitor (9) via the second switch (7); and transferring the second signal, outputted from the field effect transistor after the photoelectric conversion element and the gate of the field effect transistor are connected via the first switch, to the second capacitor (10) via the third switch (8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the noise signal removing circuit as taught by Kozuka in the solid state image pickup device of Nomura in order to improve the image quality and remove the noise from the image data.

9: Claims 18, and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,933,189 Nomura in view of USPN 5,808,677 Yonemoto in view of USPN 6,037,577 Tanaka et al.

10: As for Claim 18, Nomura in view of Yonemoto teaches the claimed invention as discussed in Claim 14. However, Nomura does not teach the use of a fourth switch for each pixel arranged between the field effect transistor and a power supply, for selecting a row.

Tanaka et al teaches in Figure 7 and on Column 9, Lines 3-24 a solid state image pickup device that has a fourth switch (3_{11}), arranged between the field effect transistor (2_{11}) and a power supply, which enables the image sensor to select a row to output the signals from pixels in a given row for selecting a row.

Therefore, it would have been obvious to on of ordinary skill in the art at the time the invention was made row selecting switch arranged between the field effect transistor (2_{11}) and a power supply as taught by Tanaka et al in the image sensor or Nomura in order to select a row to output the signals from pixels in a given row for selecting a row.

11: As for Claim 22, Nomura in view of Yonemoto teaches the claimed invention as discussed in Claim 20. However, Nomura does not teach the use of a fourth switch arranged between the field effect transistor and a power supply, for selecting a row.

Tanaka et al teaches in Figure 7 and on Column 9, Lines 3-24 a solid state image pickup device that has a fourth switch (3_{11}), arranged between the field effect transistor (2_{11}) and a power supply, which enables the image sensor to select a row to output the signals from pixels in a given row for selecting a row.

Therefore, it would have been obvious to on of ordinary skill in the art at the time the invention was made row selecting switch arranged between the field effect transistor (2_{11}) and a power supply as taught by Tanaka et al in the image sensor or Nomura in order to select a row to output the signals from pixels in a given row for selecting a row.

Allowable Subject Matter

12: Claims 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M Hannett whose telephone number is 703-305-7880. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2612

JMH
May 6, 2004

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